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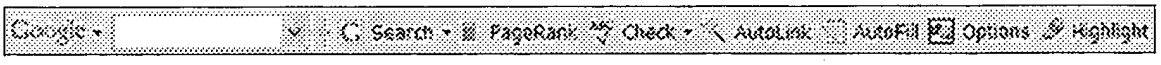

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1 Noise-tolerant design and analysis techniques: Noise characterization of static CMOS gates

Rouwaida Kanj, Timothy Lehner, Bhavna Agrawal, Elyse Rosenbaum

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(911.30 KB) Additional Information: full citation, abstract, references, index terms

We present new macromodeling techniques for capturing the response of a CMOS logic gate to noise pulses at the input. Two approaches are presented. The first one is a robust mathematical model which enables the hierarchical generation of noise abstracts for circuits composed of the precharacterized cells. The second is a circuit equivalent model which generates accurate noise waveforms for arbitrarily shaped and timed multiple-input glitches, arbitrary loads, and external noise coupling.

Keywords: cell model, circuit-equivalent model, mathematical model, noise analysis, sensitivity, simulation

2 Identification and Modeling of Nonlinear Dynamic Behavior in Analog Circuits

Xiaoling Huang, H. Alan Mantooth

February 2004 **Proceedings of the conference on Design, automation and test in Europe - Volume 1**

Full text available: pdf(151.31 KB) Additional Information: full citation, abstract, index terms

This paper presents a new approach for identifying nonlinear dynamic behavior in analog circuits. The approach facilitates the creation of models that more accurately reflect the dynamic behavior of a circuit. It has been used in a fully automated, behavioral modeling tool,Ascend, that starts from the netlist description of the circuit and generates differential algebraic equation (DAE) based behavioral models. The underlying modeling approach is overviewed to provide a context for this research ...

3 Managing leakage power: Accurate estimation of total leakage current in scaled CMOS logic circuits based on compact current modeling

Saibal Mukhopadhyay, Arijit Raychowdhury, Kaushik Roy

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(576.44 KB) Additional Information: full citation, abstract, references, citings, index terms

Dramatic increase of subthreshold, gate and reverse biased junction band-to-band-tunneling (BTBT) leakage in scaled devices, results in the drastic increase of total leakage power in a logic circuit. In this paper a methodology for accurate estimation of the total leakage in a logic circuit based on the compact modeling of the different leakage current in scaled devices has been developed. Current models have been developed based on the exact device geometry, 2-D doping profile and operating tem ...

Keywords: doping profiles, leakage, threshold voltage, tunneling

4 Session 4D: interconnect analysis: Hierarchical interconnect circuit models
Michael Beattie, Satrajit Gupta, Lawrence Pileggi
November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(179.94 KB) Additional Information: full citation, abstract, references, citings

The increasing size of integrated systems combined with deep submicron physical modeling details creates an explosion in RLC interconnect modeling complexity of unmanageable proportions. Interconnect extraction tools employ hierarchy to manage complexity, but this hierarchy is discarded via eliminating far away coupling terms when the equivalent RLC circuits are formed. The increasing dominance of capacitance coupling along with the emergence of on-chip inductance, however, makes the composite e ...

5 Substrate modeling and lumped substrate resistance extraction for CMOS ESD/latchup circuit simulation
Tong Li, Ching-Han Tsai, Elyse Rosenbaum, Sung-Mo Kang
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Full text available: pdf(846.62 KB) Additional Information: full citation, references, index terms

6 A unified signal transition graph model for asynchronous control circuit synthesis
Alexandre Yakovlev, Luciano Lavagno, Alberto Sangiovanni-Vincentelli
November 1992 **Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(1.19 MB) Additional Information: full citation, references, index terms

7 Split circuit model for test generation
Wu-Tung Cheng
June 1988 **Proceedings of the 25th ACM/IEEE conference on Design automation**
Full text available: pdf(637.28 KB) Additional Information: full citation, abstract, references, citings, index terms

Over the years, the D-algorithm has been successfully used to generate tests for sequential circuits and combinational circuits. There are 5-valued and 9-valued circuit models used for the D-algorithm. The disadvantage of a model with lower value count is its inability to assign a more precise value for a test generation requirement without some undue assumptions or decisions which may cause backtracks or even may find no test for testable faults. However, the availability ...

8 Accurate interconnect modeling: towards multi-million transistor chips as microwave circuits

N. P. van der Meijs, T. Smedes

January 1997 **Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(148.96 KB) Additional Information: full citation, abstract, references, index terms

Publisher Site

In this tutorial we discuss concepts and techniques for the accurate and efficient modeling and extraction of interconnect parasitics in VLSI designs. Due to increasing operating frequencies, microwave-like effects will become important. Therefore stronger demands are put on extraction and verification tools. We indicate the state-of-the-art for capacitance, resistance and substrate resistance extraction and discuss some open problems. We also discuss several model reduction techniques as well a ...

Keywords: Physical Design Verification, Interconnect Modeling, Interconnect Resistance Extraction, Interconnect Capacitance Extraction, Substrate Resistance Extraction

9 Delay fault models and test generation for random logic sequential circuits

T. J. Chakraborty, V. D. Agrawal, M. L. Bushnell

July 1992 **Proceedings of the 29th ACM/IEEE conference on Design automation**

Full text available: pdf(876.81 KB) Additional Information: full citation, references, citings, index terms

10 Generating efficient models for analog circuits: Scalable trajectory methods for on-demand analog macromodel extraction

Saurabh K. Tiwary, Rob A. Rutenbar

June 2005 **Proceedings of the 42nd annual conference on Design automation**

Full text available: pdf(1.10 MB) Additional Information: full citation, abstract, references, index terms

Trajectory methods sample the state trajectory of a circuit as it simulates in the time domain, and build macromodels by reducing and interpolating among the linearizations created at a suitably spaced subset of the time points visited during training simulations. Unfortunately, moving from simple to industrial circuits requires more extensive training, which creates models too large to interpolate efficiently. To make trajectory methods practical, we describe a scalable interpolation architectu ...

Keywords: SPICE, analog, circuit, macromodel, trajectory method

11 Analog macromodeling: Systematic development of analog circuit structural macromodels through behavioral model decoupling

Ying Wei, Alex Doboli

June 2005 **Proceedings of the 42nd annual conference on Design automation**

Full text available: pdf(1.33 MB) Additional Information: full citation, abstract, references, index terms

This paper presents a systematic methodology to create customized structural macromodels for a specific analog circuit. The novel contributions of the method include definition of the building block behavioral concept and two original algorithms to generate structural models. Experiments are offered for two-stage opamp and operational transconductor amplifier (OTA) circuits. The automatically

produced models are accurate, offer design insight, and require low modeling effort.

Keywords: analog circuits, structural macromodel

12 iSMILE: a novel circuit simulation program with emphasis on new device model development

A. T. Yang, S. M. Kang

June 1989 **Proceedings of the 26th ACM/IEEE conference on Design automation**

Full text available: pdf(380.61 KB) Additional Information: full citation, abstract, references, citings, index terms

The laborious task of implementing a new device model in a circuit simulator has long been recognized as a painful bottleneck to device modeling. In contrast to the conventional circuit simulators which employ a built-in model library approach, iSMILE generates and links all the necessary codes automatically from a minimal set of model descriptions contained in a user's model input file. Users are completely shielded from the internal complexity of the program when implementing n ...

13 Session 1D: Analog macromodeling: Simulation-based automatic generation of signomial and posynomial performance models for analog integrated circuit sizing

Walter Daems, Georges Gielen, Willy Sansen

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(163.89 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a method to automatically generate posynomial response surface models for the performance parameters of analog integrated circuits. The posynomial models enable the use of efficient geometric programming techniques for circuit sizing and optimization. To avoid manual derivation of approximate symbolic equations and subsequent casting to posynomial format, techniques from design of experiments and response surface modeling in combination with SPICE simulations are used to gene ...

Keywords: analog circuit modeling, design of experiments, geometric programming, posynomial and signomial response surface modeling

14 Session 4B: high-level design tools for analog circuits: Verification of delta-sigma converters using adaptive regression modeling

Jeongjin Roh, Suresh Seshadri, Jacob A. Abraham

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(116.40 KB) Additional Information: full citation, abstract, references

A new verification technique for ΔΣ analog-to-digital converters (ADC) is proposed. The ADC is partitioned into functional blocks, and adaptive regression models for each partition are constructed using transistor-level simulation data. Non-idealities in circuit behavior are captured by the adaptive regression technique from the collected data. The algorithms have been implemented in a simulation program ARSIM (Adaptive Regression Simulator), which performs data sampling, model build ...

15 Satisfiability models and algorithms for circuit delay computation

Luís Guerra e Silva, João Marques-Silva, L. Miguel Silveira, Karem A. Sakallah

January 2002 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 7 Issue 1

Full text available: pdf(270.96 KB) Additional Information: full citation, abstract, references, index terms

The existence of false paths represents a significant and computationally complex problem in the estimation of the true delay of combinational and sequential circuits. In this article we conduct a comprehensive study of modeling circuit delay computation, accounting for false paths, as a sequence of instances of Boolean satisfiability. Several path sensitization models and delay models are studied. In addition we evaluate some of the most competitive Boolean satisfiability algorithms seeking to ...

Keywords: Boolean satisfiability, circuit delay computation, delay modeling, false path, timing analysis

16 Timing abstraction: Efficient stimulus independent timing abstraction model based on a new concept of circuit block transparency

Martin Foltin, Brian Foutz, Sean Tyler

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(68.50 KB) Additional Information: full citation, abstract, references, index terms

We have developed a new timing abstraction model for digital circuit blocks that is stimulus independent, port based, supports designs with level triggered latches, and can be input into commercial STA (Static Timing Analysis) tools. The model is based on an extension of the concept of latch transparency to circuit block transparency introduced in this paper. It was implemented, tested and is being used in conjunction with transistor level STA for microprocessor designs with tens of millions of ...

Keywords: VLSI design, circuit optimization, timing analysis, timing model

17 Automated Modeling of Custom Digital Circuits for Test

S. Bose

March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(156.90 KB) Additional Information: full citation, abstract

Publisher Site

Models meant for logic verification and simulation areoften used for ATPG. For custom digital circuits, these modelscontain many tristate devices, which leads to lower faultcoverage. Unlike other research in the literature, the modelingalgorithms presented in this paper analyze each channelconnected component in the context of its environment,thereby capturing the relationship among its input signals.This reduces the number of tristates and increases the modelingefficiency, as measured by fault ...

18 A gate level model for CMOS combinational logic circuits with application to fault detection

Sudhakar M. Reddy, Vishwani D. Agrawal, Sunil K. Jain

June 1984 **Proceedings of the 21st conference on Design automation**

Full text available: pdf(467.85 KB) Additional Information: full citation, abstract, references, citings, index terms

A procedure to derive gate level equivalent circuits for CMOS combinational logic circuits is given. The procedure leads to a model containing AND, OR and NOT gates. Specifically it does not require memory elements as does an earlier model and also uses fewer gates. It is shown that tests for classical stuck-at-0 and stuck-at-1 faults in the equivalent circuit can be used to detect line stuck-at, stuck-open and stuck-on faults in the modeled CMOS circuit.

19 High frequency interconnect modeling: Vector potential equivalent circuit based on PEEC inversion

Hao Yu, Lei He

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(374.94 KB) Additional Information: full citation, abstract, references, citings, index terms

The geometry-integration based vector potential equivalent circuit (VPEC) was introduced to obtain a localized circuit model for inductive interconnects in [1]. In this paper, we show that the method in [1] is accurate only for the two body problem. We derive N-body VPEC models based on geometry integration and inversion of inductance matrix under the PEEC model, respectively. Both VPEC models are derived from first principles and are accurate compared to the full PEEC model. The resulting circu ...

20 MOS circuit models in Network C

William S. Beckett

July 1986 **Proceedings of the 23rd ACM/IEEE conference on Design automation**

Full text available: pdf(684.46 KB) Additional Information: full citation, abstract, references, citings, index terms

Network C is a programming language designed for constructing simulation models of VLSI circuits and systems. The language, which is a superset of C, supports a range of modeling capabilities including approximate solution of Kirchoff equations at the circuit level and discrete event functional simulation at the system level. When used to model a MOS circuit, the system first decomposes the circuit into a set of independent stages. The values of nodes, represented by piece-wise linear funct ...

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61 Technology mapping algorithms for domino logic

Min Zhao, Sachin S. Sapatnekar

April 2002 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 7 Issue 2

Full text available: pdf(480.59 KB) Additional Information: full citation, abstract, references, index terms

We present an efficient algorithm for technology mapping of domino logic to a parameterized library. The algorithm is optimal for mapping trees consisting of two-input AND/OR nodes, and has a computation time that is polynomial in terms of constraint size. The mapping method is then extended to DAG covering that permits the implicit duplication of logic nodes. Our synthesis procedure maps the complementary logic cones independently when AND/OR logic is to be implemented, and together using dual- ...

Keywords: Domino logic, XOR/XNOR logic, dual-monotonic gates, parameterized library, phase assignment, synthesis, technology mapping

62 Optimal Transistor Tapering for High-Speed CMOS Circuits

L. Ding, P. Mazumder

March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(157.39 KB) Additional Information: full citation, abstract

Publisher Site

Transistor tapering is a widely used technique appliedto optimize the geometries of CMOS transistors in high-performancecircuit design with a view to minimizing thedelay of a FET network. Currently, in a long series-connectedFET chain, the dimensions of the transistors aredecreased from bottom transistor to the top transistor in amanner where the width of transistors is tapered linearlyor exponentially. However, it has not been mathematicallyproved whether either of these tapering schemes yields ...

63 Constructing Symbolic Models for the Input/Output Behavior of Periodically Time-Varying Systems Using Harmonic Transfer Matrices

P. Vanassche, G. Gielen, W. Sansen

March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(199.33 KB) Additional Information: full citation, abstract
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A new technique is presented for generating symbolic expressionsfor the harmonic transfer functions of linear periodicallytime-varying (LPTV) systems, like mixers and PLL's. The algorithm,which we call Symbolic HTM, is based on the organisationof the harmonic transfer functions into a harmonic transfer matrix.This representation allows to manipulate LPTV systems in away that is similar to linear time-invariant (LTI) systems, making itpossible to generate symbolic expressions which relate the ove ...

64 Logisim: a graphical system for logic circuit design and simulation

Carl Burch

March 2002 **Journal on Educational Resources in Computing (JERIC)**, Volume 2 Issue 1

Full text available: pdf(183.47 KB) Additional Information: full citation, abstract, references, citings, index terms

Logisim enables students in introductory courses to design and simulate logic circuits. The program's design emphasizes simplicity of use, with a secondary goal of enabling design of sophisticated circuits. This motivates a two-tiered system, where users can move to the second tier by selecting a menu option.Users draw circuits of logic gates using the toolbox model popular in drawing programs. The circuit automatically propagates circuit values through the circuit; by selecting the appropriate ...

Keywords: Circuit simulation, digital logic, education

65 Interconnect Energy Dissipation in High-Speed ULSI Circuits

Payam Heydari, Massoud Pedram

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available: pdf(289.61 KB) Additional Information: full citation, abstract, citings
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This work presents accurate closed-form expressions for the interconnect energy dissipation in high-speed ULSI circuits. Unlike previous works, the energy is calculated using an approximated expression for the driving-point impedance of lossy coupled transmission lines which itself is derived by solving Telegrapher's equations. The effect of electromagnetic (inductive and capacitive) couplings on the energy dissipation is accounted for in the derivations. We synthesize a new stable circuit that ...

Keywords: Ultra-large integrated (ULSI) circuits, Interconnect, Transmission lines, Energy dissipation CMOS circuits, RLC circuits

66 Session 5B: Embedded tutorial: CAD solutions and outstanding challenges for mixed-signal and RF IC design: CAD solutions and outstanding challenges for mixed-signal and RFIC design

Domine Leenaerts, Georges Gielen, Rob A. Rutenbar

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(1.87 MB) Additional Information: full citation, abstract, references, index terms

This tutorial paper addresses the problems and solutions that are posed by the design of mixed-signal integrated systems on chip (SoC). These include problems in mixed-signal design methodologies and flows, problems in analog design productivity, as well as open problems in analog, mixed-signal and RF design, modeling and verification tools. The tutorial explains the problems that are posed by these mixed-signal/RF SoC designs, describes the solutions and their underlying methods that exist toda ...

67 Session 3D: Interconnect performance and reliability optimization: Compact modeling and SPICE-based simulation for electrothermal analysis of multilevel ULSI interconnects

Ting Yen Chiang, Kaustav Banerjee, Krishna C. Saraswat

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(157.82 KB) Additional Information: full citation, abstract, references, index terms

This paper presents both compact analytical models and fast SPICE based 3-D electro-thermal simulation methodology to characterize thermal effects due to Joule heating in high performance Cu/low-k interconnects under steady-state and transient stress conditions. The results demonstrate excellent agreement with experimental data and those using Finite Element (FE) thermal simulations (ANSYS). The effect of vias, as additional heat sinking paths to alleviate the temp erature rise in the metal wire ...

68 Session 1C: Interconnect planning: Bus encoding to prevent crosstalk delay

Bret Victor, Kurt Keutzer

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(165.72 KB) Additional Information: full citation, abstract, references, citings, index terms

The propagation delay across long on-chip buses is increasingly becoming a limiting factor in high-speed designs. Crosstalk between adjacent wires on the bus may create a significant portion of this delay. Placing a shield wire between each signal wire alleviates the crosstalk problem but doubles the area used by the bus, an unacceptable consequence when the bus is routed using scarce top-level metal resources. Instead, we propose to employ data encoding to eliminate crosstalk delay within a bus ...

69 Session2: Beyond workflow management: product-driven case handling

W. M. P. van der Aalst, P. J. S. Berens

September 2001 **Proceedings of the 2001 International ACM SIGGROUP Conference on Supporting Group Work**

Full text available: pdf(287.45 KB) Additional Information: full citation, abstract, references, citings, index terms

In the last decade, workflow technology has become one of the building blocks for realizing enterprise information systems. Unfortunately, the application of contemporary workflow management systems is limited to well-defined and well-controlled environments. In practice, workflow technology often fails because of limited flexibility. We advocate a paradigm shift to overcome this problem: Workflows should not be driven by pre-specified control-flows but by the products they generate. This paper ...

Keywords: FLOWer, case handling, product-driven design, workflow management, workflow management systems

70 Mismatch analysis and direct yield optimization by specwise linearization and feasibility-guided search

Frank Schenkel, Michael Pronath, Stephen Zizala, Robert Schwencker, Helmut Graeb, Kurt Antreich

June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(187.40 KB) Additional Information: full citation, abstract, references, citings, index terms

We present a new method for mismatch analysis and automatic yield optimization of analog integrated circuits with respect to global, local and operational tolerances. Effectiveness and efficiency of yield estimation and optimization are guaranteed by consideration of feasibility regions and by performance linearization at worst-case points. The proposed methods were successfully applied to two example circuits for an industrial fabrication process.

71 Nuts and bolts of core and SoC verification

Ken Albin

June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(164.10 KB) Additional Information: full citation, abstract, references, index terms

Digital design at Motorola is performed at design centers throughout the world, on projects with different design objectives, executed on different time scales, by different sized teams with different skill sets. This paper attempts to categorize these diverse efforts and identify common threads: what works, what the challenges are, and where we need to go.

Keywords: biased-random simulation, monitors, testbenches, verification

72 A new gate delay model for simultaneous switching and its applications

Liang-Chi Chen, Sandeep K. Gupta, Melvin A. Breuer

June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(163.26 KB) Additional Information: full citation, abstract, references, citings, index terms

73 Timing analysis with crosstalk as fixpoints on complete lattice

Hai Zhou, Narendra Shenoy, William Nicholls

June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(230.52 KB) Additional Information: full citation, abstract, references, citings, index terms

Increasing delay variation due to crosstalk has a dramatic impact on deep sub-micron technologies. It is now necessary to include crosstalk in timing analysis. But timing analysis with crosstalk is a chicken-and-egg problem since crosstalk effect in turn depends on timing behavior of a circuit. In this paper, we establish a theoretical foundation for timing analysis with crosstalk. We show that solutions to the problem are fixpoints on a complete lattice. Base on that, we prove in general t ...

74 Directed explicit model checking with HSF-SPIN

Stefan Edelkamp, Alberto Lluch Lafuente, Stefan Leue

May 2001 **Proceedings of the 8th international SPIN workshop on Model checking of software**

Full text available: pdf(249.55 KB) Additional Information: full citation, abstract, references, citings

We present the explicit state model checker HSF-SPIN which is based on the model checker SPIN and its Promela modeling language. HSF-SPIN incorporates directed search algorithms for checking safety and a large class of LTL-specified liveness properties. We start off from the A* algorithm and define heuristics to accelerate the search into the direction of a specified failure situation. Next we propose an improved nested depth-first search algorithm that exploits the structure of Promela Never ...

75 Functional test generation for behaviorally sequential models

F. Ferrandi, G. Ferrara, D. Sciuto, A. Fin, F. Fummi

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(145.75 KB) Additional Information: full citation, references, citings, index terms

76 Towards the logic defect diagnosis for partial-scan designs

Shi-Yu Huang

January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**

Full text available: pdf(12.89 MB) Additional Information: full citation, abstract, references, citings, index terms

Logical defect diagnosis is a critical yet challenging process in VLSI manufacturing. It involves the identification of the defect spots in a logic IC that fails testing. In the last decade, algorithms for diagnosis have progressed significantly and the results are showing promise for full -scan designs. In this paper, we will first review several classical algorithms such as fault dictionary based analysis and effect cause analysis. Then, we discuss several diagnosis algorithms borrowed fr ...

77 Session 1D:issues in timing estimation: Miller factor for gate-level coupling delay calculation

Pinhong Chen, Desmond A. Kirkpatrick, Kurt Keutzer

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(129.32 KB) Additional Information: full citation, abstract, references, citings

In coupling delay computation, a *Miller factor* of more than 2X may be necessary to account for active coupling capacitance when modeling the delay of deep submicron circuitry in the presence of active coupling capacitance. We propose an efficient method to estimate this factor such that the delay response of a *decoupling circuit model* can emulate the original coupling circuit. Under the assumptions of zero initial voltage, equal charge transfer, and 0.5*VDD* as the ...

78 Session 8A: static timing analysis: Switching window computation for static timing analysis in presence of crosstalk noise

Pinhong Chen, Desmond A. Kirkpatrick, Kurt Keutzer

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(88.18 KB) Additional Information: full citation, abstract, references, citings

Crosstalk effect is crucial for timing analysis in very deep submicron design. In this paper, we present and compare multiple scheduling algorithms to compute switching windows for static timing analysis in presence of crosstalk noise. We also introduce an efficient technique to evaluate the worst case alignment of multiple aggressors.

79 Session 1D:issues in timing estimation: Effects of global interconnect optimizations on performance estimation of deep submicron design

Yu Cao, Chenming Hu, Xuejue Huang, Andrew B. Kahng, Sudhakar Muddu, Dirk Stroobandt, Dennis Sylvester

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(116.06 KB) Additional Information: full citation, abstract, references, citings

In this paper, we quantify the impact of global interconnect optimization techniques that address such design objectives as delay, peak noise, delay uncertainty due to noise, power, and cost. In doing so, we develop a new system-performance simulation model as a set of studies within the MARCO GSRC Technology Extrapolation (GTX) system. We model a typical point-to-point global interconnect and focus on accurate assessment of both circuit and design technology with respect to such issues as induc ...

Keywords: VLSI, crosstalk noise, inductance, interconnect delay, system performance models, technology extrapolation

80 New enhancements to cut, fade, and dissolve detection processes in video segmentation

Ba Tu Truong, Chitra Dorai, Svetha Venkatesh

October 2000 **Proceedings of the eighth ACM international conference on Multimedia**

Full text available: pdf(733.18 KB) Additional Information: full citation, abstract, references, citings, index terms

We present improved algorithms for cut, fade, and dissolve detection which are fundamental steps in digital video analysis. In particular, we propose a new adaptive threshold determination method that is shown to reduce artifacts created by noise and motion in scene cut detection. We also describe new two-step algorithms for fade and dissolve detection, and introduce a method for eliminating false positives from a list of detected candidate transitions. In our detailed study of these gradual ...

Terms used **equivalent circuit model miller capacitance**

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Relevance scale

1 Session 1D: issues in timing estimation: Miller factor for gate-level coupling delay calculation

Pinhong Chen, Desmond A. Kirkpatrick, Kurt Keutzer

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(129.32 KB) Additional Information: full citation, abstract, references, citings

In coupling delay computation, a *Miller factor* of more than 2X may be necessary to account for active coupling capacitance when modeling the delay of deep submicron circuitry in the presence of active coupling capacitance. We propose an efficient method to estimate this factor such that the delay response of a *decoupling circuit model* can emulate the original coupling circuit. Under the assumptions of zero initial voltage, equal charge transfer, and 0.5*VDD* as the ...

2 Crosstalk noise analysis: Gate delay calculation considering the crosstalk capacitances

Soroush Abbaspour, Massoud Pedram

January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04 , Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04**

Full text available: pdf(194.52 KB) Additional Information: full citation, abstract, references
Publisher Site

In this paper, we present a new technique for calculating the output waveform of CMOS drivers for cross-coupled RC loads. The proposed technique is based on an effective capacitance calculation for each driver and an efficient, provably convergent, iteration scheme between the coupled drivers. Our technique can easily handle different input arrival times, transition times, and polarities, and can be extended to multiple cross-coupled drivers in a straightforward manner. Experimental results show ...

3 Interconnect Energy Dissipation in High-Speed ULSI Circuits

Payam Heydari, Massoud Pedram

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available: pdf(289.61 KB) Additional Information: full citation, abstract, citings
Publisher Site

This work presents accurate closed-form expressions for the interconnect energy dissipation in high-speed ULSI circuits. Unlike previous works, the energy is calculated using an approximated expression for the driving-point impedance of lossy coupled transmission lines which itself is derived by solving Telegrapher's equations. The effect of electromagnetic (inductive and capacitive) couplings on the energy dissipation is accounted for in the derivations. We synthesize a new stable circuit that ...

Keywords: Ultra-large integrated (ULSI) circuits, Interconnect, Transmission lines, Energy dissipation CMOS circuits, RLC circuits

4 A behavioral signal path modeling methodology for qualitative insight in and efficient sizing of CMOS opamps

Francky Leyn, Walter Daems, Georges Gielen, Willy Sansen

November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(159.97 KB) Additional Information: full citation, abstract, references, citings, index terms
Publisher Site

This paper describes a new modeling methodology that allows to derive systematically behavioral signal path models of operational amplifiers. Combined with symbolic simulation, these models provide high qualitative insight in the small-signal functioning of a circuit. The behavioral signal path model provides compact interpretable expressions for the poles and zeros that constitute the signal path. These expressions show which design parameters have dominant influence on the position of a pole/z ...

Keywords: behavioral signal path, incremental modeling, small-signal, minimax optimization, sequential design space pruning

5 Delay and power optimization in VLSI circuits

Lance A. Glasser, Lennox P.J. Hoyte

June 1984 **Proceedings of the 21st conference on Design automation**

Full text available: pdf(597.98 KB) Additional Information: full citation, abstract, references, citings, index terms

The problem of optimally sizing the transistors in a digital MOS VLSI circuit is examined. Macromodels are developed and new theorems on the optimal sizing of the transistors in a critical path are presented. The results of a design automation procedure to perform the optimization is discussed.

6 Noise-constrained performance optimization by simultaneous gate and wire sizing based on Lagrangian relaxation

Hui-Ru Jiang, Jing-Yang Jou, Yao-Wen Chang

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Full text available: pdf(172.58 KB) Additional Information: full citation, references, citings, index terms

7 Power supply noise analysis methodology for deep-submicron VLSI chip design

Howard H. Chen, David D. Ling

June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**

Full text available: pdf(237.07 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

This paper describes a new design methodology to analyzethe on-chip power supply noise for high-performance microprocessors.Based on an integrated package-level andchip-level power bus model, and a simulated switching circuitmodel for each functional block, this methodology offersthe most complete and accurate analysis of Vdd distributionfor the entire chip. The analysis results not only providedesigners with the inductive ¿I noise and the resistive IRdrop data at the same time, but also allow d ...

8 The analog behavior of digital integrated circuits

Lance A. Glasser

June 1981 **Proceedings of the 18th conference on Design automation**

Full text available: pdf(674.15 KB) Additional Information: full citation, abstract, references, citings, index terms

The analog behavior of digital VLSI circuits is investigated. A theory based on nonlinear Thevenin equivalent circuits and RC ladder networks is developed. We obtain closed form expressions for the upper and lower bounds on propagation delay through a string of inverters. We generalize this to multiple-input, multiple-output gates and show that the problem of estimating signal propagation delays in VLSI circuits may be reduced to the problem of summing the step responses of a set of linear ...

9 VLSI Circuits: Active shields: a new approach to shielding global wires

Himanshu Kaul, Dennis Sylvester, David Blaauw

April 2002 **Proceedings of the 12th ACM Great Lakes symposium on VLSI**

Full text available: pdf(114.12 KB) Additional Information: full citation, abstract, references, citings, index terms

A new shielding scheme, active shielding, is proposed for reducing delays on interconnects. As opposed to conventional (passive) shielding, the active shielding approach helps to speed up signal propagation on a wire by ensuring in-phase switching of adjacent nets. Results show that the active shielding scheme improves performance by up to 16% compared to passive shields and up to 29% compared to unshielded wires. When signal slopes at the end of the line are compared, savings of up to 38% and 2 ...

10 Noise-tolerant design and analysis techniques: Noise characterization of static CMOS gates

Rouwaida Kanj, Timothy Lehner, Bhavna Agrawal, Elyse Rosenbaum

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(911.30 KB) Additional Information: full citation, abstract, references, index terms

We present new macromodeling techniques for capturing the response of a CMOS logic gate to noise pulses at the input. Two approaches are presented. The first one is a robust mathematical model which enables the hierarchical generation of noise abstracts for circuits composed of the precharacterized cells. The second is a circuit equivalent model which generates accurate noise waveforms for arbitrarily shaped and timed multiple-input glitches, arbitrary loads, and external noise coupling.

Keywords: cell model, circuit-equivalent model, mathematical model, noise analysis, sensitivity, simulation

11 A hardware engine for analogue mode simulation of MOS digital circuits

David M. Lewis

June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation**

Full text available: pdf(803.41 KB) Additional Information: full citation, abstract, references, index terms

Purely digital simulators that model digital circuits by approximations often produce poor results with even simple circuits. Analogue simulators, however, are far more accurate than necessary for digital circuits and correspondingly expensive to use. We argue that an analogue simulation is necessary, but that a simple enough approximation can be used to allow a hardware simulation engine to perform the calculations. The critical features of such an engine are discussed here, its performanc ...

12 Advanced design and modeling techniques: Piecewise quadratic waveform matching with successive chord iteration

Zhong Wang, Jianwen Zhu

January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04 , Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair ASP-DAC '04**

Full text available: pdf(132.90 KB) Additional Information: full citation, abstract, references

Publisher Site

While fast timing analysis methods based on model order reduction have been well established for linear circuits, the timing analysis for non-linear circuits, which are dominant in digital circuits, is usually performed by a SPICE-like, numerical integration-based approach solving differential equations. In this paper, we propose a new technique that leads to the transient so lution of charge/discharge paths with a complexity equivalent to only *K* DC operating point calculations, where ...

13 Symbolic Parasitic Extractor for Circuit Simulation (SPECS)

J. D. Bastian, M. Ellement, P. J. Fowler, C. E. Huang, L. P. McNamee

June 1983 **Proceedings of the 20th conference on Design automation**

Full text available: pdf(620.41 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes the design, development and implementation of the program SPECS. The purpose of SPECS is to automatically extract from a Rockwell microelectronic symbolic matrix description a netlist for circuit simulation. This program differs from others in that it uses a symbol layout matrix as an input, calculates both interelectrode and intrinsic capacitance, calculates conductor resistance, produces a schematic representation of the network and has a selective TRACE, i.e., traces ...

14 Automatic circuit analysis based on mask information

B. T. Preas, B. W. Lindsay, C. W. Gwyn

June 1976 **Proceedings of the 13th conference on Design automation**

Full text available: pdf(769.12 KB) Additional Information: full citation, abstract, references, citings, index terms

A Circuit MAsk Translator (CMAT) code has been developed which converts integrated circuit mask information into a circuit schematic. Logical operations, pattern recognition, and special functions are used to identify and interconnect diodes, transistors, capacitors, and resistances. The circuit topology provided by the translator is compatible with the input required for a circuit analysis program.

15 Switch-Factor Based Loop RLC Modeling for Efficient Timing Analysis

Yu Cao, Xiao-dong Yang, Xuejue Huang, Dennis Sylvester

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(169.38 KB) Additional Information: full citation, abstract, index terms

Timing uncertainty caused by inductive and capacitivecoupling is one of the major bottlenecks in timing analysis. In thispaper, we propose an effective loop RLC modeling technique toefficiently decouple lines with both inductive and capacitivecoupling. We generalize the RLC decoupling problem based ontransmission line theory and a switch-factor, which is the voltageratio between two nets. This switch-factor is also known as theMiller factor and is widely used to model capacitive coupling.The pro ...

Keywords: RLC model, loop inductance, switch-factor, current return loop, static timing analysis, slew rate, data-bus, and clock

16 Optimal P/N width ratio selection for standard cell libraries

David S. Kung, Ruchir Puri

November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(195.26 KB) Additional Information: full citation, abstract, references, citings, index terms

The effectiveness of logic synthesis to satisfy increasingly tight timing constraints in deep-submicron high-performance circuits heavily depends on the range and variety of logic gates available in the standard cell library. Primarily, research in the design of high-performance standard cell libraries has been focused on drive strength selection of various logic gates. Since CMOS logic circuit delays not only depend on the drive strength of each gate but also on its P/N width ratio, it is ...

17 Session 5: Interconnect and Architecture Planning: Global interconnect trade-off for technology over memory modules to application level: case study

A. Papanikolaou, M. Miranda, F. Catthoor, H. Corporaal, H. De Man, D. De Roest, M. Stucchi, Karen Maex

April 2003 **Proceedings of the 2003 international workshop on System-level interconnect prediction**

Full text available: pdf(180.30 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper we show how to exploit energy-delay trade-offs that exist due to the variation of the technology parameters for the implementation of interconnect wires. We also evaluate how these trade-offs can be propagated to the memory module level, so we can minimise the power consumption of the entire memory organisation (i.e., memories and connections between them). Our approach is that at future technology nodes the delay problem can be handled at the application level, so given any delay ...

Keywords: Pareto-optimal energy/delay interconnect exploration, interconnect wire processing, intra/inter-memory interconnect

18 Special session: hierarchical design and design space exploration of analog integrated circuits: Deterministic approaches to analog performance space exploration (PSE)

Daniel Mueller, Guido Stehr, Helmut Graeb, Ulf Schlichtmann

June 2005 **Proceedings of the 42nd annual conference on Design automation**

Full text available: pdf(256.58 KB) Additional Information: full citation, abstract, references, index terms

Performance space exploration (PSE) determines the range of feasible performance values of a circuit block for a given topology and technology. In this paper, we present two deterministic approaches for PSE. One approximates the feasible performance space based on linearized circuit models and is suitable for investigating a large number of performances. The other one computes discretizations of the Pareto front of competing performances. In addition, a motivation and application of PSE using a ...

Keywords: analog integrated circuits, fourier motzkin elimination, pareto optimization, performance space exploration

19 Weibull Based Analytical Waveform Model

Chirayu S. Amin, Florentin Dartu, Yehea I. Ismail

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(255.51 KB) Additional Information: full citation, abstract, index terms

Current CMOS technologies are characterized by interconnectlines with increased relative resistance w.r.t. driver outputresistance. Designs generate signal waveshapes that are verydifficult to model using a single parameter model such as thetransition time. In this paper, we present a simple and robustparameter analytical expression for waveform modeling based onthe Weibull cumulative distribution function. The Weibull modelaccurately captures the variety of waveshapes without introducingsignifi ...

20 A unified framework for race analysis of asynchronous networks

J. A. Brzozowski, C.-J. Seger

January 1989 **Journal of the ACM (JACM)**, Volume 36 Issue 1

Full text available: pdf(2.11 MB) Additional Information: full citation, abstract, references, citings, index terms, review

A unified framework is developed for the study of asynchronous circuits of both gate and MOS type. A basic network model consisting of a directed graph and a set of vertex excitation functions is introduced. A race analysis model, using three values (0, 1, and x), is developed for studying state transitions in the network. It is shown that the results obtained using this model are equivalent to those using ternary simulation. It is also proved that the set of state variables can be reduced ...

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1 Rendering: Efficient modeling and rendering of turbulent water over natural terrain

Nathan Holmberg, Burkhard C. Wünsche

June 2004 **Proceedings of the 2nd international conference on Computer graphics and interactive techniques in Australasia and Southe East Asia**

Full text available: pdf(403.82 KB) Additional Information: full citation, abstract, references, index terms

Water phenomena are some of the most visually spectacular effects found in nature. This paper presents an efficient hybrid method to model turbulent water such as fast flowing rivers and waterfalls with the intent that the model can be used as part of a larger environment or scene. The model presented uses hydrostatic theory to incorporate a 2D height field and a particle system to model respectively the main volume and spray of turbulent water. The user is able to submit any environment formed ...

Keywords: physically-based modeling, turbulent water, water simulation

2 Military applications: Simulation analysis: applications of discrete event simulation modeling to military problems

Raymond R. Hill, J. O. Miller, Gregory A. McIntyre

December 2001 **Proceedings of the 33nd conference on Winter simulation**

Full text available: pdf(390.01 KB) Additional Information: full citation, abstract, references, index terms

The military is a big user of discrete event simulation models. The use of these models range from training and wargaming their constructive use in important military analyses. In this paper we discuss the uses of military simulation, the issues associated with military simulation to include categorizations of various types of military simulation. We then discuss three particular simulation studies undertaken with the Air Force Institute of Technology's Department of Operational Science focused ...

3 Modeling leadership effects and recruit type in an Army recruiting station

Edward L. McLarney, J. O. Miller, Kenneth W. Bauer, Robert Fancher

December 1999 **Proceedings of the 31st conference on Winter simulation: Simulation---a bridge to the future - Volume 2**

Full text available: pdf(95.73 KB) Additional Information: full citation, references, citings, index terms

4 Performance modeling of database and simulation protocols: design choices for query driven simulation
John A. Miller, Nancy D. Griffeth
April 1991 **Proceedings of the 24th annual symposium on Simulation**
Full text available: pdf(1.26 MB) Additional Information: full citation, references, citings, index terms

5 Session 1D:issues in timing estimation: Miller factor for gate-level coupling delay calculation
Pinhong Chen, Desmond A. Kirkpatrick, Kurt Keutzer
November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(129.32 KB) Additional Information: full citation, abstract, references, citings

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6 Modeling software design diversity: a review
Bev Littlewood, Peter Popov, Lorenzo Strigini
June 2001 **ACM Computing Surveys (CSUR)**, Volume 33 Issue 2
Full text available: pdf(259.57 KB) Additional Information: full citation, abstract, references, citings, index terms

Design diversity has been used for many years now as a means of achieving a degree of fault tolerance in software-based systems. While there is clear evidence that the approach can be expected to deliver some increase in reliability compared to a single version, there is no agreement about the extent of this. More importantly, it remains difficult to evaluate exactly how reliable a particular diverse fault-tolerant system is. This difficulty arises because assumptions of independence of fai ...

Keywords: *N*-version software, control systems, functional diversity, multiple version programming, protection systems, safety, software fault tolerance

7 SIGSAM BULLETIN: Computer algebra in the life sciences
Michael P. Barnett
December 2002 **ACM SIGSAM Bulletin**, Volume 36 Issue 4
Full text available: pdf(240.15 KB) Additional Information: full citation, abstract, references

This note (1) provides references to recent work that applies computer algebra (CA) to the life sciences, (2) cites literature that explains the biological background of each application, (3) states the mathematical methods that are used, (4) mentions the benefits of CA, and (5) suggests some topics for future work.

8 Computerization of the workplace: testing attitudinal effects with a causal model
Urs E. Gattiker, Todd Nelligan, Rosemarie S. Gattiker, Cynthia Cunningham

October 1986 **Proceedings of the twenty-second annual computer personnel research conference on Computer personnel research conference**

Full text available: pdf(1.12 MB) Additional Information: full citation, abstract, references, citings

This paper examines various aspects of computerization and their effects upon quality of work life in organizations. An integrative model was developed which views quality of work life as an ever changing dimension influenced not only by computerization, but, also, by perception of career success as well as non-work factors. Evaluation of gathered data supported the model in that workers experiencing computerization positively were more likely to exhibit organizational commitment. Furthermo ...

9 PocketLens: Toward a personal recommender system

Bradley N. Miller, Joseph A. Konstan, John Riedl

July 2004 **ACM Transactions on Information Systems (TOIS)**, Volume 22 Issue 3

Full text available: pdf(1.10 MB) Additional Information: full citation, abstract, references, index terms

Recommender systems using collaborative filtering are a popular technique for reducing information overload and finding products to purchase. One limitation of current recommenders is that they are not portable. They can only run on large computers connected to the Internet. A second limitation is that they require the user to trust the owner of the recommender with personal preference data. Personal recommenders hold the promise of delivering high quality recommendations on palmtop computers, e ...

Keywords: Collaborative Filtering, Peer-to-Peer Networking, Privacy, Recommender Systems

10 Switch-Factor Based Loop RLC Modeling for Efficient Timing Analysis

Yu Cao, Xiao-dong Yang, Xuejue Huang, Dennis Sylvester

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(169.38 KB) Additional Information: full citation, abstract, index terms

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Keywords: RLC model, loop inductance, switch-factor, current return loop, static timing analysis, slew rate, data-bus, and clock

11 Effects of participative management on the performance of software development teams

Woo Young Chung, Patricia J. Guinan

April 1994 **Proceedings of the 1994 computer personnel research conference on Reinventing IS : managing information technology in changing organizations: managing information technology in changing organizations**

Full text available: pdf(649.05 KB) Additional Information: full citation, abstract, references, citings, index terms

Researchers and practitioners advocate a participative management style for improving employee productivity and job satisfaction. Field studies have shown that participation has a modest, yet positive influence on productivity and job satisfaction. For software development teams, however, management approaches such as the notion of the chief programmer suggest that participation might not be productive. Systematic research has not been conducted to investigate the importance of a participat ...

12 Noise-tolerant design and analysis techniques: Noise characterization of static CMOS gates

Rouwaida Kanj, Timothy Lehner, Bhavna Agrawal, Elyse Rosenbaum

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(911.30 KB) Additional Information: full citation, abstract, references, index terms

We present new macromodeling techniques for capturing the response of a CMOS logic gate to noise pulses at the input. Two approaches are presented. The first one is a robust mathematical model which enables the hierarchical generation of noise abstracts for circuits composed of the precharacterized cells. The second is a circuit equivalent model which generates accurate noise waveforms for arbitrarily shaped and timed multiple-input glitches, arbitrary loads, and external noise coupling.

Keywords: cell model, circuit-equivalent model, mathematical model, noise analysis, sensitivity, simulation

13 Session 1D:issues in timing estimation: Effects of global interconnect optimizations on performance estimation of deep submicron design

Yu Cao, Chenming Hu, Xuejue Huang, Andrew B. Kahng, Sudhakar Muddu, Dirk Stroobandt, Dennis Sylvester

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(116.06 KB) Additional Information: full citation, abstract, references, citings

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Keywords: VLSI, crosstalk noise, inductance, interconnect delay, system performance models, technology extrapolation

14 A study of smoothing methods for language models applied to information retrieval

Chengxiang Zhai, John Lafferty

April 2004 **ACM Transactions on Information Systems (TOIS)**, Volume 22 Issue 2

Full text available: pdf(296.22 KB) Additional Information: full citation, abstract, references, index terms

Language modeling approaches to information retrieval are attractive and promising because they connect the problem of retrieval with that of language model estimation, which has been studied extensively in other application areas such as speech recognition. The basic idea of these approaches is to estimate a language model for each document, and to then rank documents by the likelihood of the query according to the estimated language model. A central issue in language model estimation is *smo* ...

Keywords: *Dirichlet prior smoothing, EM algorithm, Jelinek--Mercer smoothing, Statistical language models, TF-IDF weighting, absolute discounting smoothing, backoff smoothing, interpolation smoothing, leave-one-out, risk minimization, term weighting, two-stage smoothing*

15 A new gate delay model for simultaneous switching and its applications
Liang-Chi Chen, Sandeep K. Gupta, Melvin A. Breuer
June 2001 **Proceedings of the 38th conference on Design automation**
Full text available: pdf(163.26 KB) Additional Information: full citation, abstract, references, citings, index terms

16 The effects of interactive graphics and text on social influence in computer-mediated small groups
Jozsef A. Toth
October 1994 **Proceedings of the 1994 ACM conference on Computer supported cooperative work**
Full text available: pdf(1.48 MB) Additional Information: full citation, abstract, references, index terms

Computer-mediated small group research has focused efforts on the medium of electronically networked text-based messages. An experiment which instead combines a synchronous text-based messaging medium with two-dimensional interactive computer graphics is detailed. Three-person groups participated in a risk-taking choice-dilemma task involving a discussion of the dilemma and consensus attainment. The groups' prediscussion and postdiscussion opinions were collected. Two conditions, one where ...

Keywords: computer-mediated small group, discourse analysis, human factors, interactive computer graphics, perceptual and cognitive persistence, small group decision-making, social influence

17 The role of computer system models in performance evaluation
Stephen R. Kimbleton
July 1972 **Communications of the ACM**, Volume 15 Issue 7
Full text available: pdf(502.00 KB) Additional Information: full citation, abstract, references, citings

Models constitute a useful means of investigating computer system performance. This paper examines the interrelationships between models and other methods for evaluating the performance of computer systems and establishes circumstances under which the use of a model is appropriate.

Keywords: analytic-models, evaluation, modeling, performance, simulation-models, system-models

18 Infinite-source, ample-server control variate models for fininte-source, finite-server repairable item systems
Mohamed A. Ahmed, Douglas R. Miller
December 1986 **Proceedings of the 18th conference on Winter simulation**
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A new modeling idea for comparing infinite-source, ample-server models (∞/∞) and finite-source, finite-server models (f/f) is considered. This comparison provides an estimate of the error when approximating an f/f system with an ∞/∞ system, and allows analytical solutions of the ∞/∞ model to be used as control variates. This approach is applied to estimate the difference in performance between an M/G/∞ queueing system (∞/∞) and the class ...

19 Technical correspondence

CORPORATE Tech Correspondence
October 1989 **Communications of the ACM**, Volume 32 Issue 10

Full text available: pdf(2.15 MB) Additional Information: full citation, references, citings, index terms

20 Clock rate versus IPC: the end of the road for conventional microarchitectures

Vikas Agarwal, M. S. Hrishikesh, Stephen W. Keckler, Doug Burger
May 2000 **ACM SIGARCH Computer Architecture News , Proceedings of the 27th annual international symposium on Computer architecture**, Volume 28 Issue 2

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The doubling of microprocessor performance every three years has been the result of two factors: more transistors per chip and superlinear scali ng of the processor clock with technology generation. Our results show that, due to both diminishing improvements in clock rates and poor wire scaling as semiconductor devices shrink, the achievable performance growth of conventional microarchitectures will slow substantially. In this paper, we describe technology-driven models for wire cap ...

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